

**Course Name**: DIGITL LOGIC DES LAB

**Course Number and Section**: **14:332:233:01**

**Experiment**: Laboratory 2: Analysis and Synthesis of Combinational Circuits

**Lab Instructor**: ZAHRA AREF

**Date Performed**: 10/4/2024

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**Course Name**: \_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_

**Course Number and Section**: **14:332:xxx:xx**

**! Important: Please include this page in your report if the submission is a paper submission. For electronic submission (email or Sakai) please omit this page.**

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GRADE: \_\_\_\_\_\_\_\_\_\_\_\_\_\_\_

COMMENTS:

**Lab2 Pre-Lab**

1. Purpose / Introduction / Overview – describe the problem and provide background information:
   1. The objectives of this prelab are to synthesize, simulate, and analyze logic functions. This first section will be dedicated to the Pre-Lab, while the second section will be the lab report.
2. Approach / Method – the approach took, how problems were solved:
   1. The logic function F(A, B, C, D) = ∑(1,3,5,6,7,14) are given in the prelab. First, a K-map and truth table must be derived from these outputs. Using this k-map the minimal sum-of-products must also be found by grouping the outputs. Then, a NAND – NAND logic diagram for the function must be drawn. Finally, this function is simulated in Verilog to display the RTL and timing diagrams.
3. Results – present your data and analysis, experimental results, etc
   1. **Circuit Minimization** 
      1. Karnaugh map for function F:

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| AB/CD | 00 | 01 | 11 | 10 |
| 00 | 0 | 1 | 1 | 0 |
| 01 | 0 | 1 | 1 | 1 |
| 11 | 0 | 0 | 0 | 1 |
| 10 | 0 | 0 | 0 | 0 |

* + 1. Minimal Sum-of-Product for F:
       1. The minimal Sum-of-Products are circled above in red. The expression is **F=A’D+BCD’**
    2. NAND-NAND Implementation of F:
    3. Truth Table for Function F:

|  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- |
| A | B | C | D | A'D | BCD' | A'D + BCD' |
| 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| 0 | 0 | 0 | 1 | 1 | 0 | 1 |
| 0 | 0 | 1 | 0 | 0 | 0 | 0 |
| 0 | 0 | 1 | 1 | 1 | 0 | 1 |
| 0 | 1 | 0 | 0 | 0 | 0 | 0 |
| 0 | 1 | 0 | 1 | 1 | 0 | 1 |
| 0 | 1 | 1 | 0 | 0 | 1 | 1 |
| 0 | 1 | 1 | 1 | 1 | 0 | 1 |
| 1 | 0 | 0 | 0 | 0 | 0 | 0 |
| 1 | 0 | 0 | 1 | 0 | 0 | 0 |
| 1 | 0 | 1 | 0 | 0 | 0 | 0 |
| 1 | 0 | 1 | 1 | 0 | 0 | 0 |
| 1 | 1 | 0 | 0 | 0 | 0 | 0 |
| 1 | 1 | 0 | 1 | 0 | 0 | 0 |
| 1 | 1 | 1 | 0 | 0 | 1 | 1 |
| 1 | 1 | 1 | 1 | 0 | 0 | 0 |

* 1. **Verilog and Simulation**
     1. Elaborated Schematic Diagram of F: A computer diagram of a computer network

        Description automatically generated with medium confidence
     2. 2 μs Behavioral Simulation Waveform: A screenshot of a computer

        Description automatically generated
     3. Timing hazard in F:
        1. The timing hazard in F is circled in blue in the K-Map.
  2. **Analysis of A Simple Combinational Circuit**
     1. Function H(A, B, C, D) Boolean Expression and Truth Table:

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| A | B | C | D | A'D |
| 0 | 0 | 0 | 0 | 0 |
| 0 | 0 | 0 | 1 | 1 |
| 0 | 0 | 1 | 0 | 0 |
| 0 | 0 | 1 | 1 | 1 |
| 0 | 1 | 0 | 0 | 0 |
| 0 | 1 | 0 | 1 | 1 |
| 0 | 1 | 1 | 0 | 0 |
| 0 | 1 | 1 | 1 | 1 |
| 1 | 0 | 0 | 0 | 0 |
| 1 | 0 | 0 | 1 | 0 |
| 1 | 0 | 1 | 0 | 0 |
| 1 | 0 | 1 | 1 | 0 |
| 1 | 1 | 0 | 0 | 0 |
| 1 | 1 | 0 | 1 | 0 |
| 1 | 1 | 1 | 0 | 0 |
| 1 | 1 | 1 | 1 | 0 |

1. Conclusion / Summary – what was done and how it was done

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